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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,274	06/19/2003	Alberto Baroncelli	B-322	6437

802 7590 02/09/2005

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EXAMINER

CHUNG, DANIEL J

ART UNIT	PAPER NUMBER
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2672

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/601,274

Applicant(s)

BARONCELLI ET AL.

Examiner

Daniel J Chung

Art Unit

2672

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 8-23-04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Information Disclosure Statement

Receipt is acknowledged of Applicant's Information Disclosure Statement of 8-23-2004, which has been placed in the application file and considered by the Examiner.

Drawings

The drawings are not objected to by the Examiner.

Claim Objections

Claim 11 is missing in the presented application. Claims 1-10 and 12-15 are presented for examination. Appropriate correction is required.

Specification

Please review the application and correct all informalities.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10 and 12-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Koselj et al (US 2003/0214506).

Regarding claim 1, Koselj et al discloses that the claimed feature of a vector graphics circuit for rendering vector and bitmap graphics objects to a final image, the vector graphics circuit comprising: a. an input display list means [10] for receiving an input stream of data (See Fig 1, Fig 2, Fig 21); b. a sorting hardware circuit for optimizing the scan conversion algorithm (See Fig 17, [11]); c. a Bezier hardware circuit [11] for vector curve subdivision (See Fig 1-2, Fig 7-8, Fig 17, Fig 21, [48],[91],[138-141], claim 24); d. an antialiasing hardware circuit for calculating sub-pixel values (See [26],[32-40],[96]); e. a color hardware circuit [7] for reordering and for optimizing the access to a plurality of bitmaps and mathematical tables inside the display list memory (See Fig 1, Fig 17, Fig 21); f. a dump buffer [13,15,17] hardware circuit, using a memory, which composes the vector graphics objects in a final pixel bitmap. (See Fig 1, Fig 17, Fig 21, [93],[244],[247])

Regarding claim 2, Koselj et al discloses that the input display list means is arranged to include a quadratic or cubic Bezier edge data list. (See Fig 7, [138-141])

Regarding claim 3, Koselj et al discloses that the input display list means is arranged to include a color data list. (See [30-32],[89],[93],[247])

Regarding claim 4, Koselj et al discloses that the input display list means is arranged to include a color ramp data list. (See [30-32],[89],[93],[247])

Regarding claim 5, Koselj et al discloses that the input display list means is arranged to include a pattern or bitmap data list. (See [7-8],[213])

Regarding claim 6, Koselj et al discloses that the sorting hardware circuit comprises: a. an active edge processor subunit that stores the edges of a current scan line inside an active edge table with increasing X, the active edge table comprises a dual port memory, where two alternating ping-pong buffers are stored; b. a free active edge stack acting as a LIFO stack, to generate the address of the active edge table. (See Fig 1, Fig 17, Fig 21)

Regarding claim 7, Koselj et al discloses that a Bezier hardware circuit store a series of segments inside an dual port memory comprising: a. a subdivided Bezier parameter unit, comprising three couples of X and Y adders/divide by two, plus a delay element; b. a De Casteljau subdivision unit; c. a Bezier subdivision tree address unit that generates the address locations of the Bezier segments inside a dual port memory. (See Fig 1-2, Fig 7-8, Fig 17, Fig 21, [48],[91],[138-141], claim 24)

Regarding claim 8, Koselj et al discloses that the antialiasing hardware circuit computes the number of sub-pixels present in a $N=i*4$ real pixels per clock, to obtained the weight factor used for a scan-converted row. (See [33],[96])

Regarding claim 9, Koselj et al discloses that the color hardware circuit includes:
a. a color generator sub unit that outputs a solid or a processed color when a linear gradient, a radial gradient a tiled bitmap or a clipped bitmap are associated with the active edge (See Fig 9-10, [151-156]); b. a color composer sub unit that uses the weight factor to process the color from the color generator and store the result in to a dump buffer. (See [93],[244],[247])

Regarding claim 10, Koselj et al discloses that the buffer hardware circuit stores a pixel region into a buffer, where all the objects are composed, comprising: a. a fixed single line dump buffer memory that stores the color pixels processed by an antialiasing and transparence factors; b. a store buffer memory that stores the color pixel value using the following algorithm: i. Read the background pixel from the store buffer memory, multiply it by the complementary of the transparence ($1-\alpha$), obtained from the dump buffer, and add it with the red, green, blue values again from the dump buffer. ii. The result is written again inside the store buffer. (See Fig 1, Fig 17, Fig 21, [151])

Regarding claim 12, claim 12 is similar in scope to the claim 7, and thus the rejection to claim 7 hereinabove is also applicable to claim 12.

Regarding claim 13, claim 13 is similar in scope to the claim 7, and thus the rejection to claim 7 hereinabove is also applicable to claim 13.

Regarding claim 14, claim 14 is similar in scope to the claim 7, and thus the rejection to claim 7 hereinabove is also applicable to claim 14.

Regarding claim 15, claim 15 is similar in scope to the combination of claims 1-10, and thus the rejections to claims 1-10 hereinabove are also applicable to claim 15.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Chung whose telephone number is (703) 306-3419. He can normally be reached Monday-Thursday and alternate Fridays from 7:30am- 5:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael, Razavi, can be reached at (703) 305-4713.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:


(703) 872-9306 (Central fax)

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

djc
February 2, 2005



**MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600**